UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,579	03/25/2004	Michael Karl Gschwind	AUS920031084US1	7116

			EXAMINER
45327	7590	08/21/2006	GU, SHAWN X

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ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>25 March 2004</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-25</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-25</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>25 March 2004</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Objection

1.   Claims 2, 3, 22 and 23 are objected to because of the following informalities:

In line 1 of both claims, it would be more appropriate to replace "where" with

"wherein". Appropriate correction is required.

Claim Rejections - 35 USC § 101

2.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

3.   Claim 24 is rejected under 35 U.S.C. 101 because the claimed invention is

directed to non-statutory subject matter. The claimed invention is a computer program

product, which has a medium with a computer program. However, the computer

program product itself is not stored in any tangible medium such as a hard disk or RAM.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

5.   Claims 1-14, 17 and 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claims 1-13 and 23, the limitation "said memory" on lines 11 and 16-17 in claim 1 and the limitation "said means for requesting for delivery" on lines 17-18 in claim 1 lack sufficient antecedent basis.

Per claims 14-22, it is unclear to the Examiner what the intended metes and bounds are of the limitation "supporting the presence of prefetch buffers" on lines 2-3 in claim 14. The term "supporting" seems to suggest anything and everything that does not prohibit the actions of occurring.

Per claim 17, the limitation "the processor core" on line 2 lacks sufficient antecedent basis.

All dependent claims are rejected as having the same deficiencies as the claims they depend from. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 14, 15, 17, 21, 22, 24 and 25 are rejected under 35 U.S.C. 103(a) as

being unpatentable over Patterson and Hennessy [Computer Architecture: A

Quantitative Approach] (hereinafter "Patterson") and Williams et al. [US 6,993,630 B1]

(hereinafter "Williams").

Per claims 14, 24 and 25, Patterson teaches a method implementing a

distributed ("directory entries can be distributed along with the memory", see page 679,

paragraph 4) directory based coherence protocol (see page 679-685, and Figs 8.22,

8.23, 8.24 and 8.25), comprising:

requesting a memory block from a memory hierarchy level having a coherence

directory and associated directory data (cache, memory and directory, see page 680,

Fig.8.22),

generating a response including memory data and coherence information

(messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the

memory data request must also be serviced as well, see page 682, last paragraph),

updating directory information (tracking the state of each cache block and coherence information related to processors sharing the blocks, see page 680; also see page 682, last paragraph),

receiving a response including memory data and coherence information from said memory hierarchy level (messages sent among nodes to maintain coherence, see page 681 and Fig.8.23, the memory data request must also be serviced as well, see page 682, last paragraph),

a testing step to indicate whether received coherence information is compatible with required access mode and a step of performing coherence actions if said test indicates one of incompatibility, and possible incompatibility (the state transitions in Figs 8.24 and 8.25 and explanations paragraphs in page 683, 684 and 685 illustrate updating the directory to enforce coherency as accesses of difference access modes are requested. For instance page 685 describes when a block is in Exclusive state, three possible coherence actions are performed when the coherence information is not compatible with the required access mode),

a step of providing data which has been obtained to a requestor of memory data (messages sent to satisfy the request, see page 682, last paragraph).

Patterson does not specifically disclose a coherence protocol "supporting the presence of prefetch buffers", a memory hierarchy level having prefetch address registers, and indicating the address of a prefetched block in a prefetch address register.

However, Williams teaches a method implementing a directory based coherence protocol supporting the presence of prefetch buffers (Secondary Level Cache 108, see Williams, Figs 1-3), a memory hierarchy level having prefetch address registers (General Register Array 300, see Williams, Fig.3, Col.9, lines 60-67 and Col.10, lines 4-40), and indicating the address of a prefetched block in a prefetch address register (GRA 300 contains the prefetch request address, see Williams, Col.9, lines 56-67 and Col.10, lines 4-59). The motivation presented by Williams for incorporating the above limitations is reducing the latency associated with data retrieval (see Williams, Col.6, lines 63-66). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to include Williams' limitations with Patterson's teachings for the same motivation described by Williams.

It is also clear that claims 24 and 25 are already substantially described by claim 14. Although Patterson does not specifically disclose computer program product or compute code implementing the limitations, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that complicated protocol algorithms such as the one described by Patterson in claim 14 should be implemented as a program product including computer code for advantages such as more flexible adaptability and scalability, easier debugging and upgrading, and lesser cost of implementation over hardware implementation.

Per claim 15, Patterson in view of Williams further teaches that providing coherence information provides separate coherence directory information and prefetch

address information (The prefetch address information is separate from the coherence

directory information described in claim 14; see Williams, Col.9, Lines 56-67 and Col.10,

Lines 12-59; the prefetch address information is provided to another processor that

requests data in the shared memory area through the bus controller 114).

Per claim 17, Patterson in view of Williams further teaches that the method

obtains a first data unit (see Williams, Fig.3, First-Level Cache 203 in Instruction

Processor 110A) for processing in the processor core, and at least one additional data

unit for storage (see Williams, Fig.3, Cache Memory 214) in said prefetch buffer.

Per claim 21, Patterson further teaches that requests and responses are

performed by sending and receiving data over logical point to point links (the messages

and replied data values are sent between the processors and the directories, with a

single source and a single destination, hence point-to point links; see page 681, lines 5-

16 and Fig. 8.23).

Per claim 22, Patterson in view of Williams further teaches at least one prefetch

address register stores at least a prefetch address and a prefetch data length (address

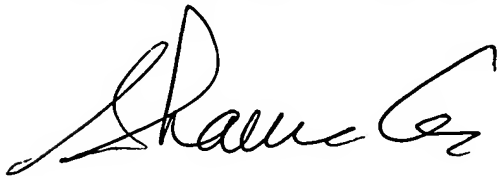and data signals are stored in GRA, see Williams, Col.9, lines 59-65).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.
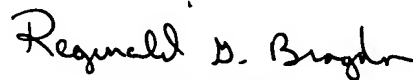
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
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17 August 2006